REMARKS

Claims 1-20 remain in the present application. Claims 1, 3, 6-7, 10, 13 and 17 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the arguments set forth below.

Claim Rejections – 35 U.S.C. §103

Claims 1-16

Claims 1-16 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over United States Patent Number 5,994,937 to Hara et al. (referred to herein as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (referred to herein as "Kwon"), further in view of United States Patent Number 6,031,366 to Mitsuishi (referred to herein as "Mitsuishi"), and further in view of United States Patent Number 6,388,490 to Saeki (referred to herein as "Saeki"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-16 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising:

> an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a first circuit for providing a selectable amount of pull down current, wherein said plurality of selectively-activated components are of a different component type than components of said first circuit for providing a selectable amount of pull down current, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal that is inversely proportional to said temperature.

Claims 2-9 depend from independent Claim 1 and recite further elements of the claimed invention.

Applicants respectfully direct the Examiner to independent Claim 10, which recites an electronic device comprising a timer circuit, wherein the timer circuit comprises:

an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, wherein said plurality of selectively-activated components are of a different component type than components of said first circuit for providing a selectable amount of pull down current, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal that is inversely proportional to said temperature, and wherein said reference signal is derived from a band gap reference circuit.

Claims 11-16 depend from independent Claim 10 and recite further elements of the claimed invention.

Applicants respectfully submit that one of ordinary skill in the art would not be motivated to modify Hara with the Figure 3 of Mitsuishi and Saeki in the claimed fashion. For example, although page 3 of the rejection states that one

would be motivated to modify Hara with the variable current source of Mitsuishi "for the purpose of saving cost," Applicants respectfully submit that replacing the Hara's single transistor 414 (Figure 4) with a plurality of transistors as shown in Mitsuishi's Figure 3 would increase cost instead of saving cost as suggested by the rejection. Further, Hara teaches a single transistor 414 which is not variable, thereby teaching away from a variable current source as taught by Mitsuishi. Accordingly, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine Hara with Mitsuishi in the claimed fashion as there is no suggestion in either reference for such a combination.

Additionally, page 3 of the rejection states that one of ordinary skill in the art would be motivated to replace Hara's inverter 402 with Saeki's capacitors "CAP11" through "CAP15" (Figure 3) "for the purpose of having more flexibility of controlling the delay of the signal outputted by the delay stage." Applicants fail to find such a motivation for combining the cited references in either Hara or Saeki, and thus, respectfully request that the Examiner point to a specific portion of either reference that supports such a motivation to combine or withdraw the rejection. Regardless, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to replace an inverter as taught by Hara with a plurality of capacitors as taught by Saeki since each component performs different functions, e.g., capacitors as taught by Saeki do not invert a signal like Hara's inverter 402. Accordingly, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine Hara with Saeki in the claimed fashion.

Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the limitations of "wherein components of said first circuit are placed in a fixed state during manufacturing" as recited in Claim 3. As recited and described in the present application, a pull-down path coupled to an output stage includes a first circuit for providing a selectable amount of pull down current. Components of the first circuit are placed in a fixed state during manufacturing. For example, the components of the first circuit may be fusible links, metal options, bond options, etc.

In contrast to the claimed embodiments, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest components placed in a fix state during manufacturing as claimed. Instead, Mitsuishi teaches a variable current source for a DA converter, where digital signals for controlling the amount of current output by the variable current source are determined during operation of the DA converter (col. 1, lines 10-18). Further, Mitsuishi teaches that the variable current source is for compensating for variations caused during manufacture. Therefore, Mitsuishi teaches varying the current during operation (e.g., after manufacture), thereby teaching away from components that are placed in a fixed state during manufacture as claimed. Accordingly, Applicants reiterate that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the limitations of "wherein components of said first circuit are placed in a fixed state during manufacturing" as recited in Claim 3.

For these reasons, Applicants respectfully submit that independent Claims 1 and 10 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since Claims 2-9 and 11-16 recite further elements of the invention claimed in their respective independent claims, Claims 2-9 and 11-16 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-16 are allowable.

Claims 17-20

Claims 17-20 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 17-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;
> during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and

during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further elements of the claimed invention.

Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the elements of "during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit," "during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage," and "during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit" as recited in independent Claim 17.

As recited and described in the present application, a timer circuit may be placed in a configuration mode and an operation mode. While in the configuration mode, configuration bits are set to control the delay through the timer circuit by determining an amount of elements coupled to the output stage of the timer circuit. Additionally, while in the configuration mode, a second set of

configuration bits are set during configuration to control an amount of pull-down current of the timer circuit. Further, when placed in the operation mode, the delay of the timer circuit is varied inversely proportional to a temperature of the timer circuit.

In contrast to the claimed embodiments, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest a plurality of distinguishable modes as claimed. Additionally, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest such a plurality of distinguishable modes comprising a configuration mode and an operation mode as claimed.

Further, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest setting a plurality of configuration bits to control pull down current *during configuration* (as opposed to during operation) as claimed. For example, even if Mitsuishi's switches and transistors as depicted in Figure 3 of Mitsuishi were added to Hara's circuit depicted in Figure 4 of Hara, neither reference teaches or suggests that adjustment of the switches are performed *during a configuration mode* as claimed.

Accordingly, Applicants reiterate that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest the limitations of "during configuration of said timer circuit, setting a first plurality of configuration bits which control the

amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit," "during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage," and "during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit" as recited in independent Claim 17.

Furthermore, page 7 of the rejection fails to direct Applicants to specific portions of the cited references which support the rejection of independent Claim 17. Applicant wishes to respectfully remind the Examiner that "the examiner should set forth in the Office action: (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate" and "(B) the difference or differences in the claim over the applied reference(s)" (MPEP §706.02(j)). Therefore, Applicants respectfully request appropriate correction to the rejection pertaining to Claim 17 in the next Office Action if the rejection is to be maintained.

For these reasons, Applicants respectfully submit that independent Claim 17 is not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since Claims 18-20 recite further elements of the invention claimed in

independent Claim 17, Claims 18-20 also overcome the 35 U.S.C. §103(a) rejection of record. Therefore, Claims 17-20 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 9 / 2 / 2008

/BMF/

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